FIG. 1A

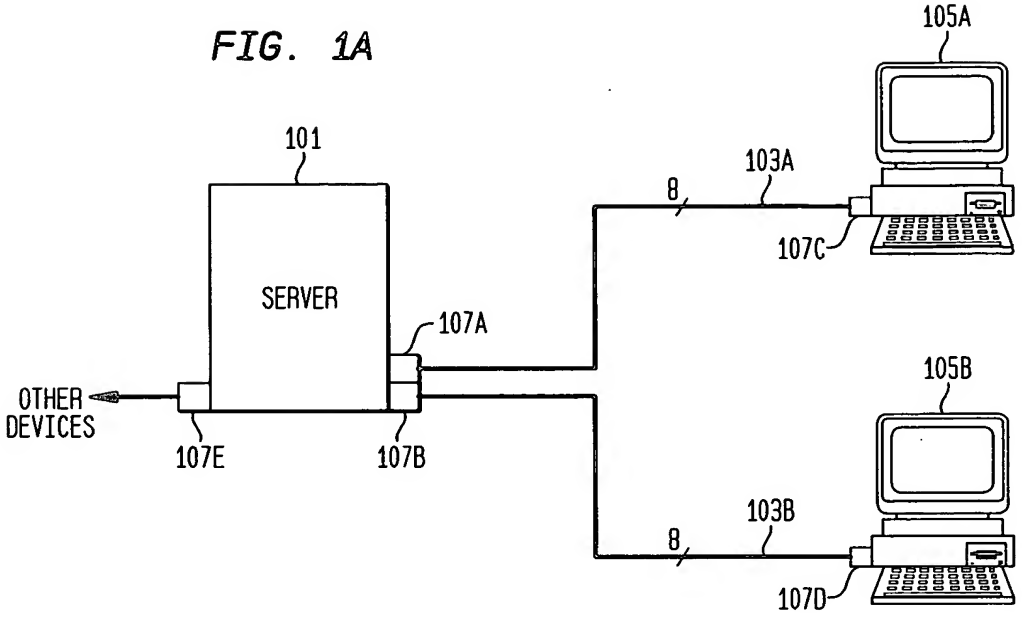
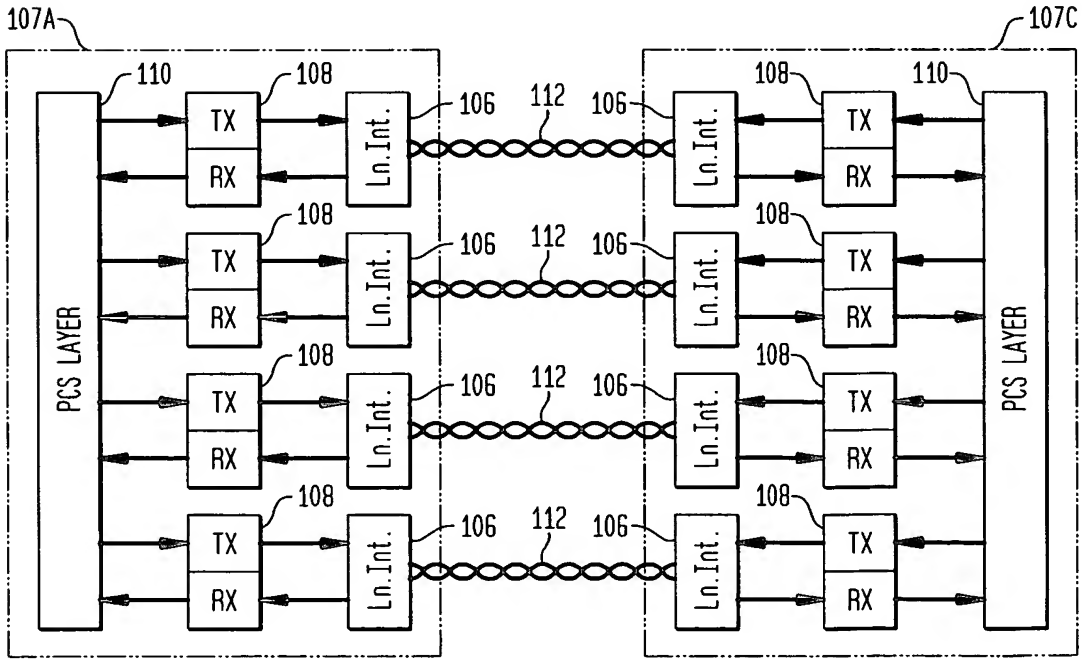

105A
101
103A
8
SERVER
107C
107A
105B
OTHER DEVICES
107E
107B
103B
8
107D

FIG. 1B


107A
107C
110
108
TX
RX
Ln.Int.
106
112
PCS LAYER

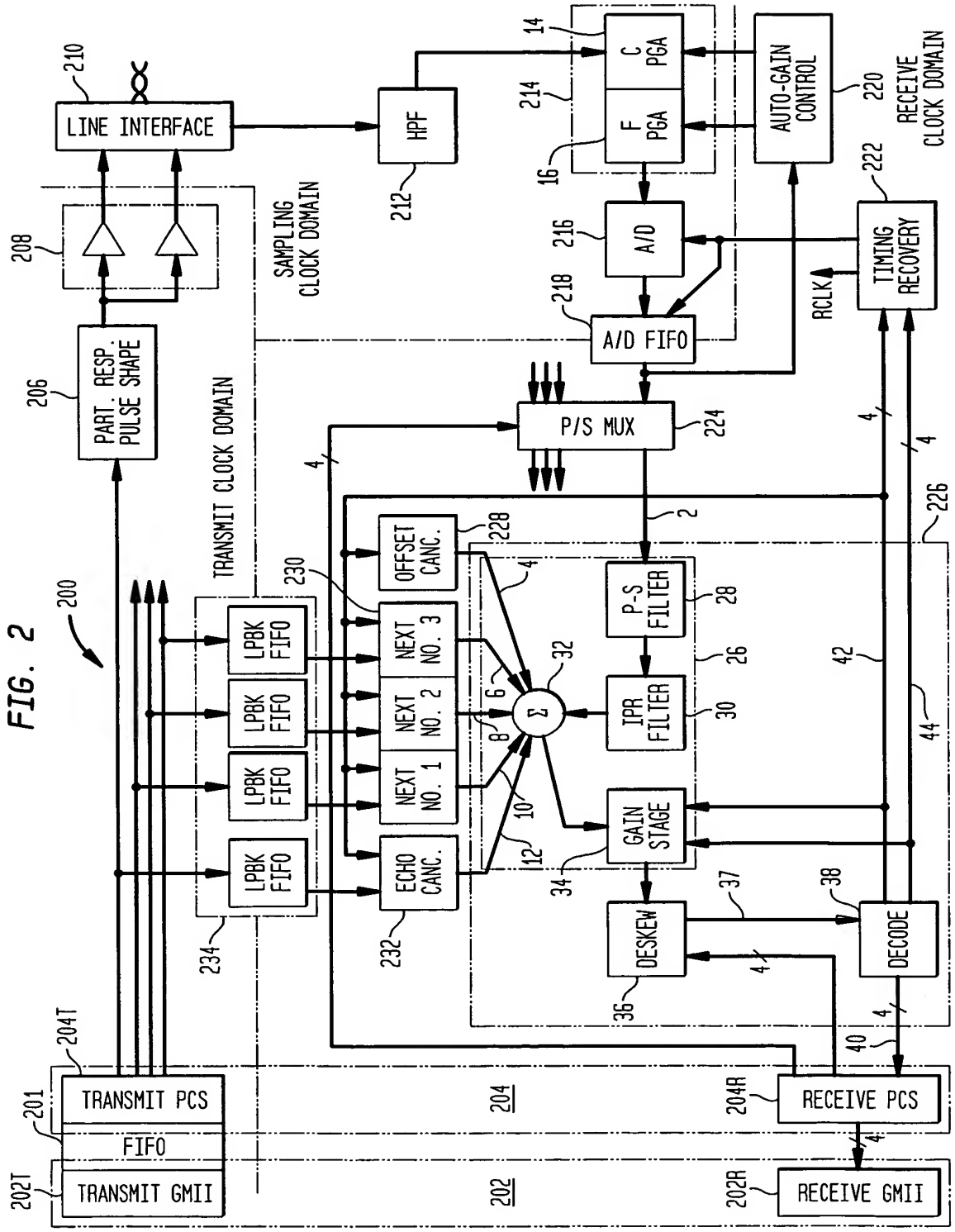

LINE INTERFACE
HPF
C PGA
F PGA
AUTO-GAIN CONTROL
RECEIVE CLOCK DOMAIN
SAMPLING CLOCK DOMAIN
A/D
TIMING RECOVERY
RCLK
A/D FIFO
PART. RESP. PULSE SHAPE
TRANSMIT CLOCK DOMAIN
P/S MUX
OFFSET CANC.
LPBK FIFO
NEXT NO. 3
NEXT NO. 2
NEXT NO. 1
ECHO CANC.
P-S FILTER
IPR FILTER
GAIN STAGE
DESKEW
DECODE
TRANSMIT PCS
FIFO
TRANSMIT GMII
RECEIVE PCS
RECEIVE GMII
FIG. 2

FIG. 3

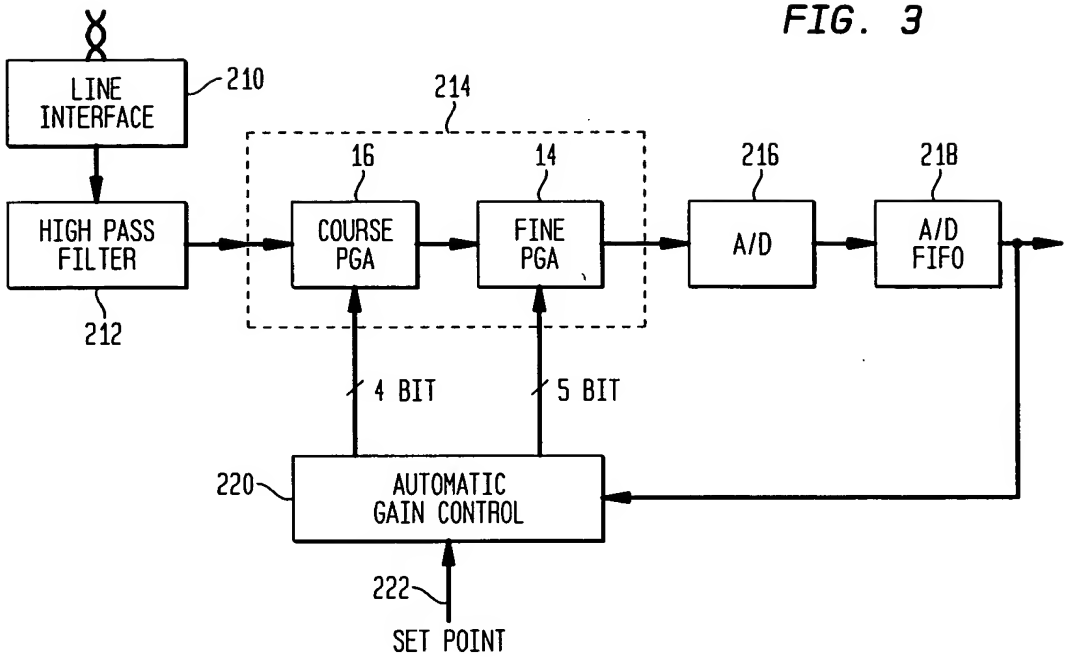

LINE INTERFACE
210
214
16
14
216
218
HIGH PASS FILTER
COURSE PGA
FINE PGA
A/D
A/D FIFO
212
4 BIT
5 BIT
220
AUTOMATIC GAIN CONTROL
222
SET POINT

FIG. 4

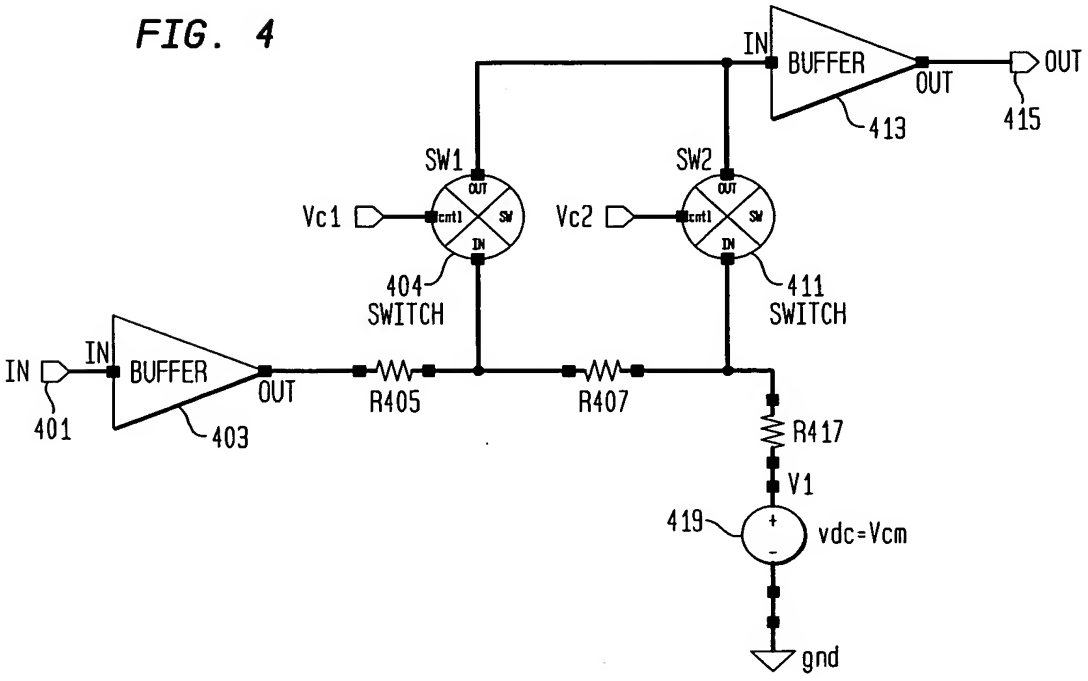

IN
BUFFER
OUT
OUT
413
415
SW1
SW2
Vc1
Vc2
cntl
SW
IN
404
SWITCH
411
SWITCH
IN
IN
BUFFER
OUT
401
403
R405
R407
R417
V1
419
vdc=Vcm
gnd

FIG. 5

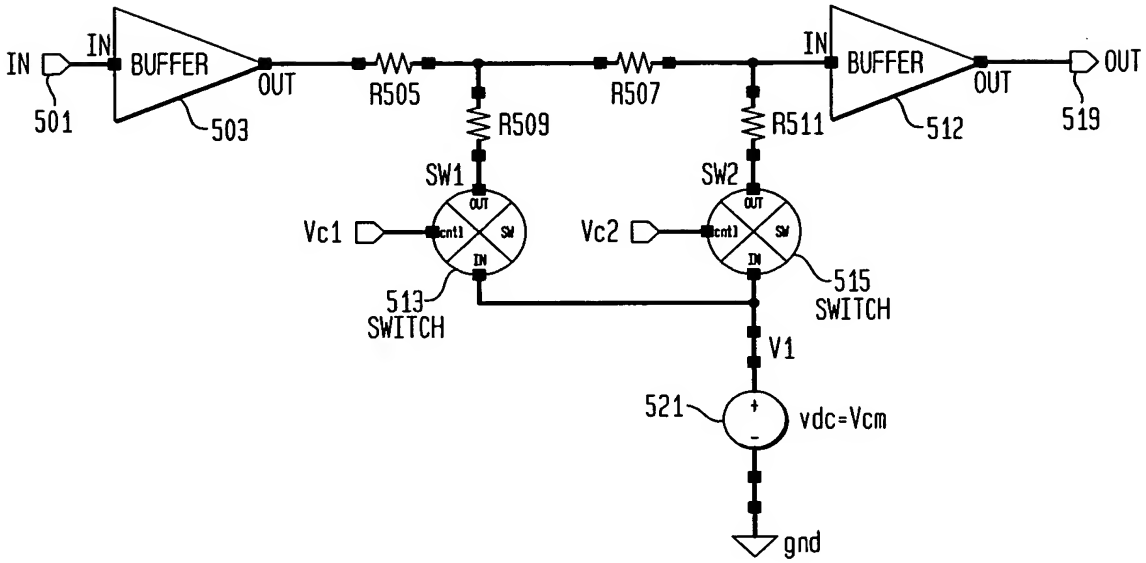

IN
IN
BUFFER
OUT
501
503
R505
R509
R507
IN
BUFFER
OUT
OUT
512
519
R511
SW1
SW2
OUT
cntl
SW
IN
Vc1
Vc2
513
SWITCH
515
SWITCH
V1
521
vdc=Vcm
gnd

FIG. 6

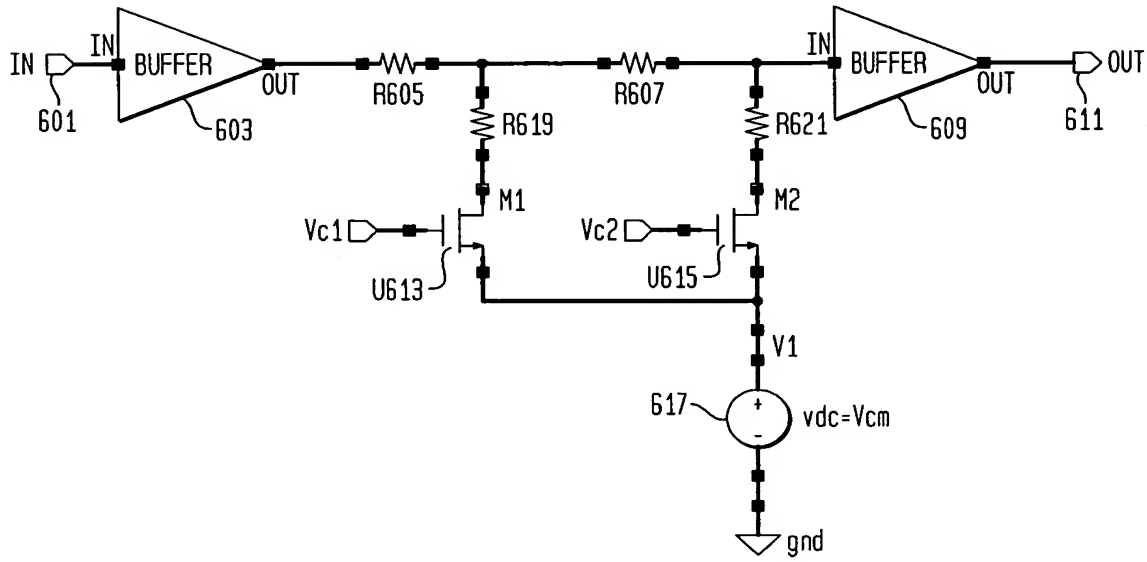

IN
IN
BUFFER
OUT
601
603
R605
R619
R607
IN
BUFFER
OUT
OUT
609
611
R621
M1
M2
Vc1
Vc2
U613
U615
V1
617
vdc=Vcm
gnd

FIG. 7

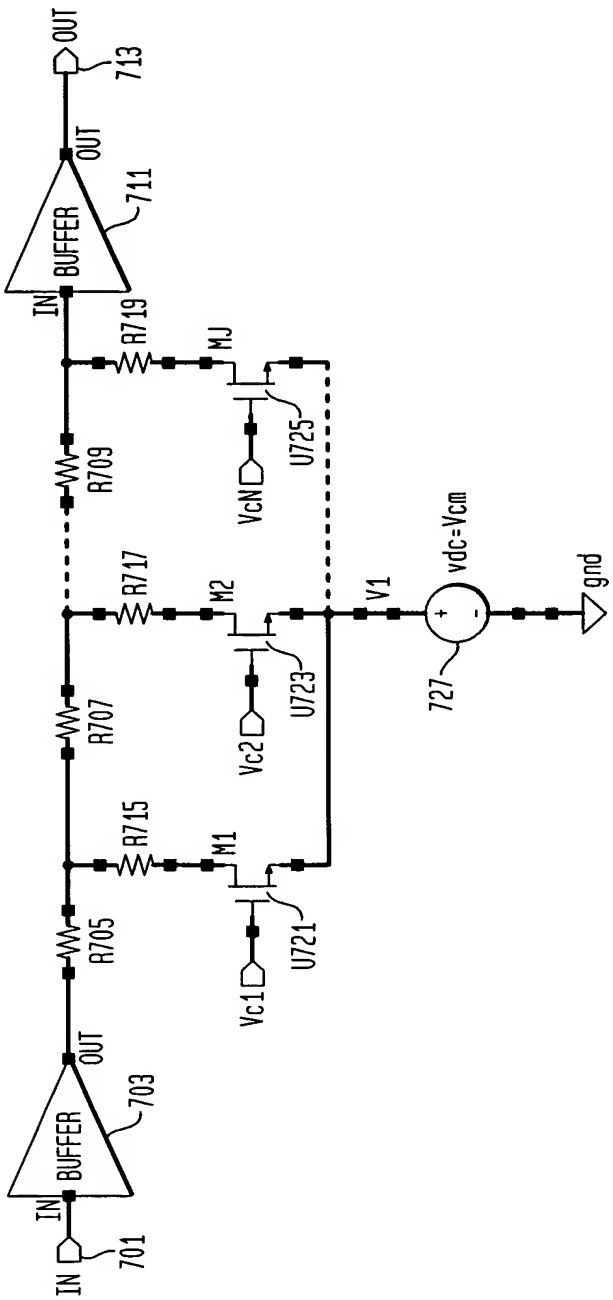

OUT
713
OUT
BUFFER
711
IN
R719
MJ
R709
U725
VcN
R717
M2
V1
vdc=Vcm
gnd
U723
Vc2
727
R707
R715
M1
R705
U721
Vc1
OUT
BUFFER
703
IN
IN
701

FIG. 8

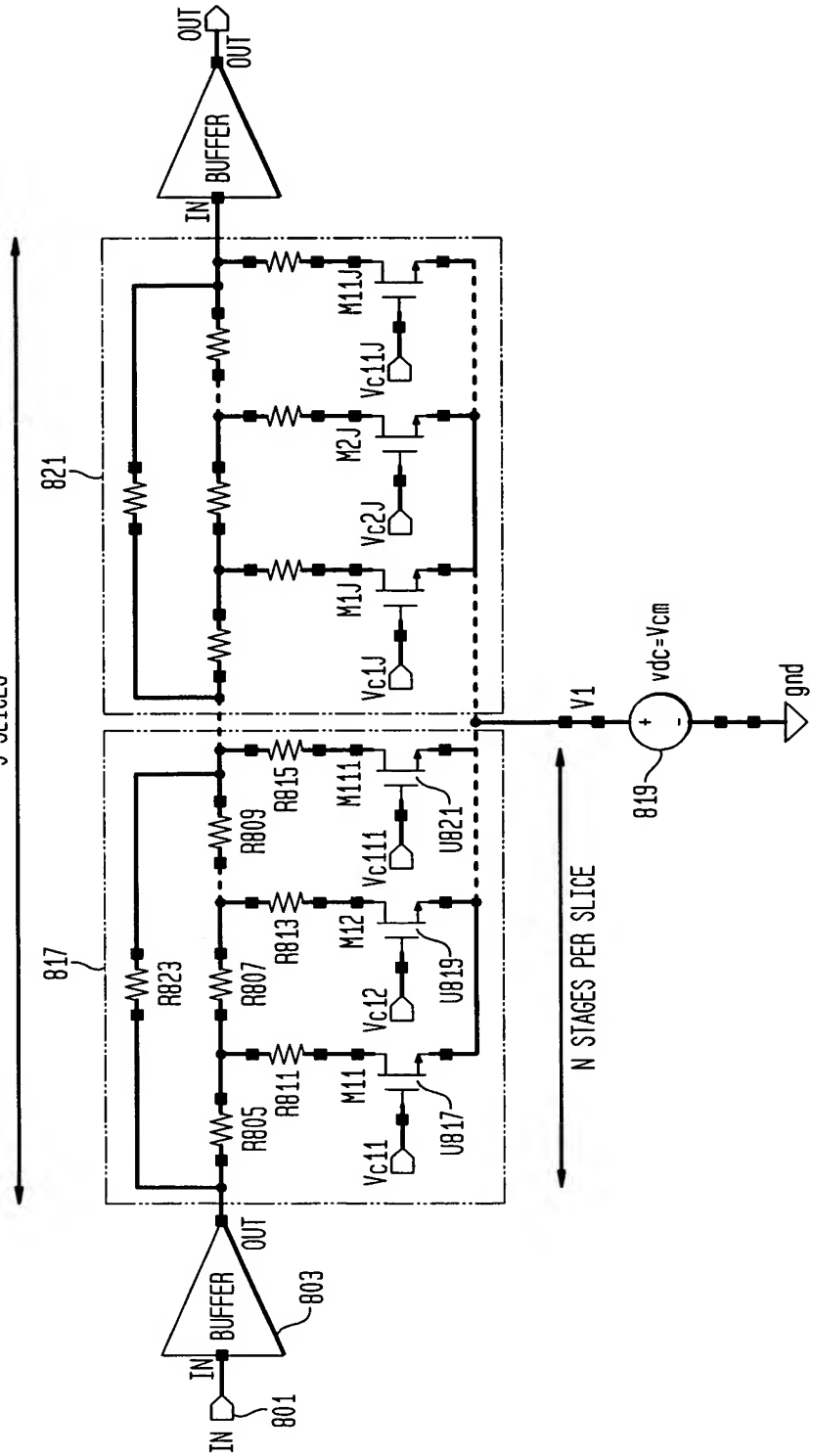

OUT
OUT
BUFFER
IN
J SLICES
821
M11J
Vc11J
M2J
Vc2J
M1J
Vc1J
V1
vdc=Vcm
gnd
819
N STAGES PER SLICE
817
R823
R809
R815
M111
Vc111
UB21
R807
R813
M12
Vc12
UB19
R805
R811
M11
Vc11
UB17
OUT
BUFFER
803
IN
IN
801

FIG. 9
(PRIOR ART)

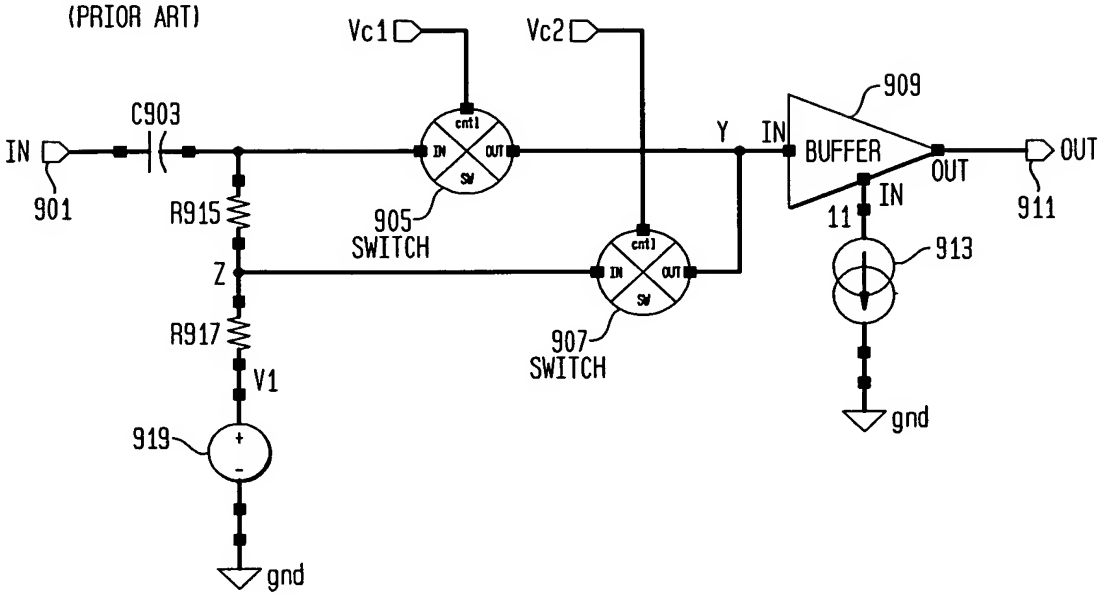


FIG. 10
(PRIOR ART)

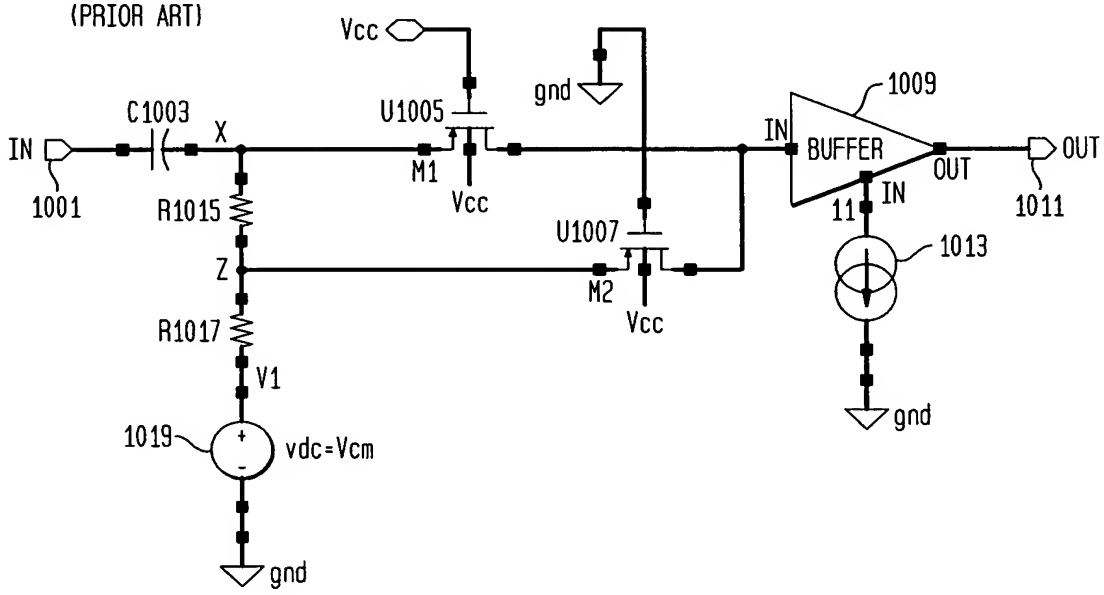


FIG. 11

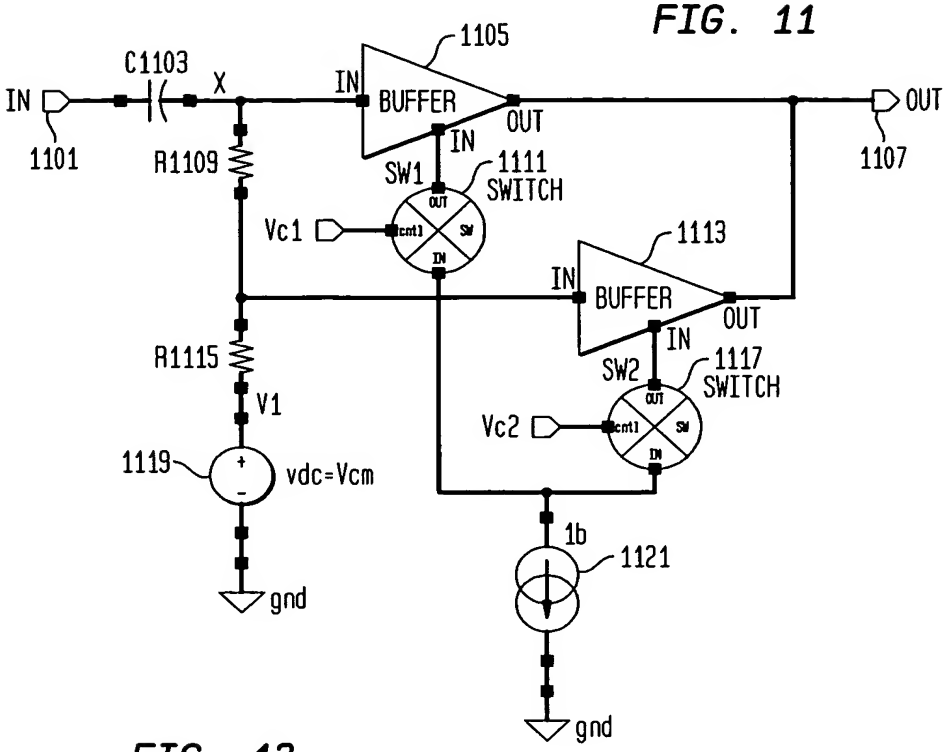

1105
C1103
X
IN
BUFFER
OUT
IN
OUT
1101
R1109
1107
SW1
1111
SWITCH
Vc1
cntl
SW
IN
1113
IN
BUFFER
OUT
IN
R1115
SW2
1117
SWITCH
V1
Vc2
1119
vdc=Vcm
1b
1121
gnd
gnd

FIG. 12

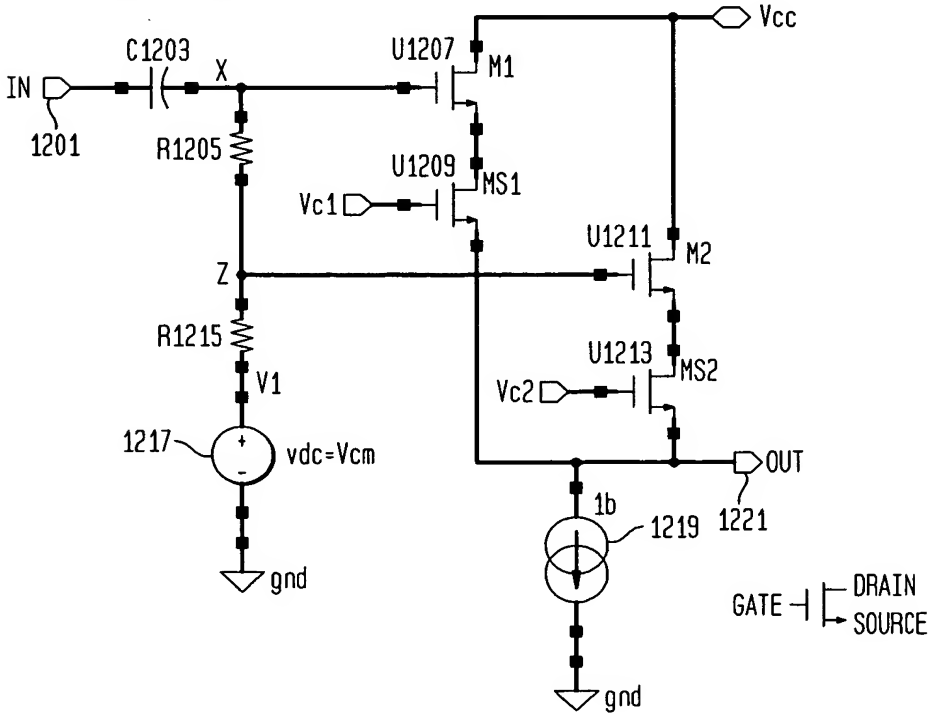
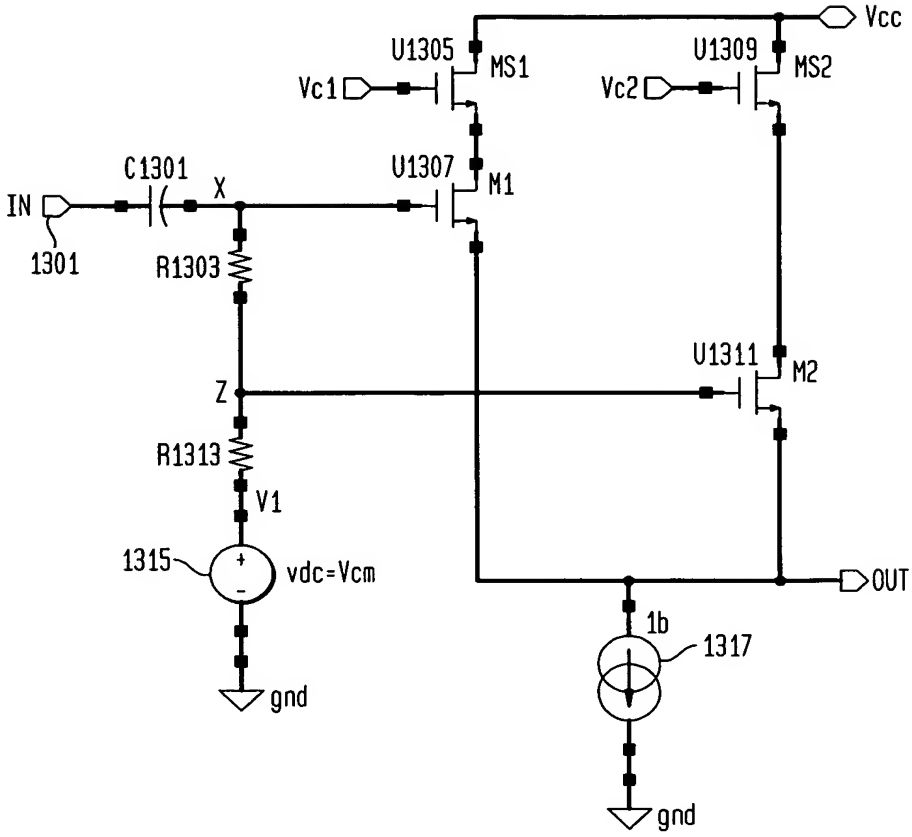

Vcc
C1203
X
U1207
M1
IN
1201
R1205
U1209
MS1
Vc1
U1211
M2
Z
R1215
U1213
MS2
V1
Vc2
1217
vdc=Vcm
OUT
1b
1219
1221
gnd
GATE
DRAIN
SOURCE
gnd

FIG. 13


Vcc
U1305
MS1
U1309
MS2
Vc1
Vc2
C1301
U1307
M1
IN
X
1301
R1303
U1311
M2
Z
R1313
V1
1315
vdc=Vcm
OUT
1b
1317
gnd
gnd

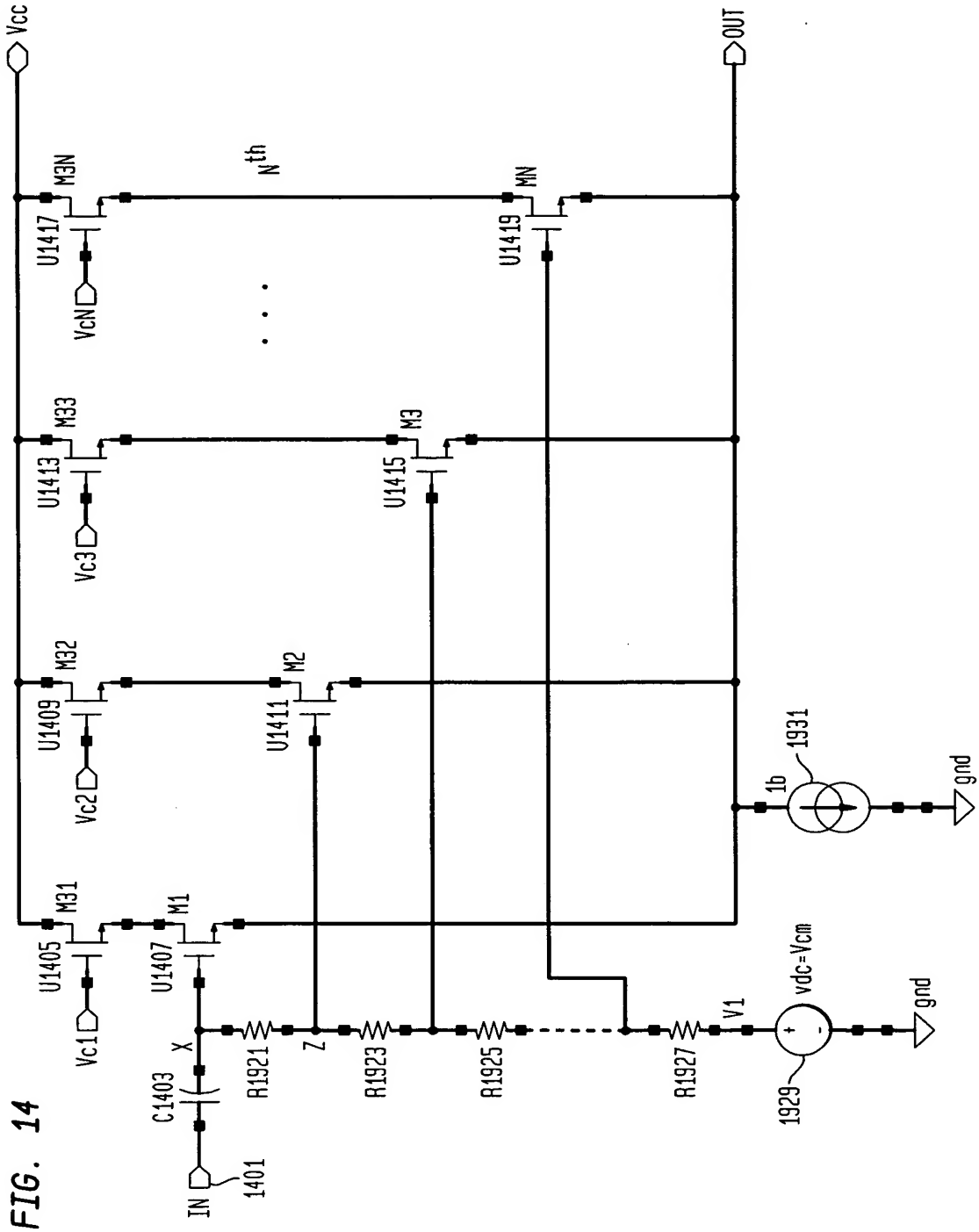

Vcc
OUT
M3N
Nth
MN
U1417
U1419
VcN
M33
M3
U1413
U1415
Vc3
M32
M2
U1409
U1411
Vc2
1b
1931
gnd
M31
M1
U1405
U1407
Vc1
X
C1403
R1921
Z
R1923
R1925
R1927
V1
vdc=Vcm
gnd
1929
IN
1401

FIG. 14

FIG. 15

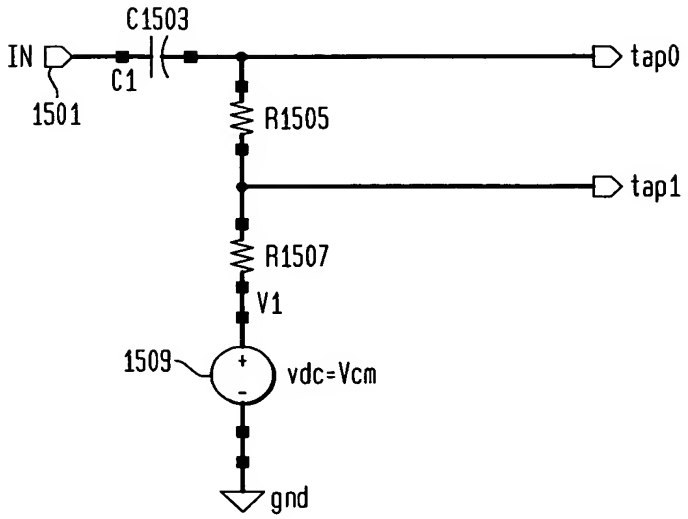

C1503
IN
C1
1501
tap0
R1505
tap1
R1507
V1
1509
vdc=Vcm
gnd

FIG. 16

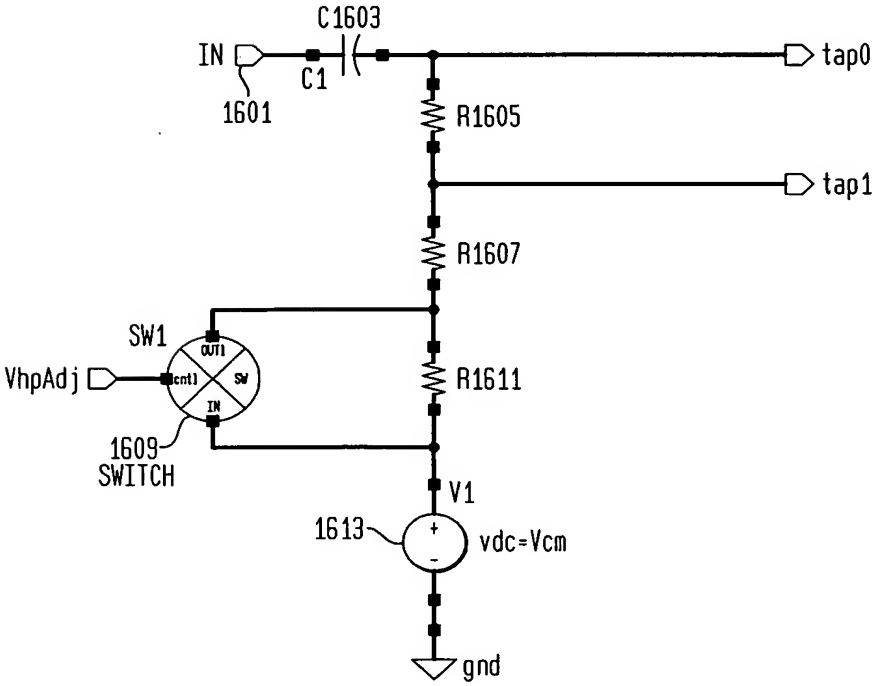

C1603
IN
C1
1601
tap0
R1605
tap1
R1607
SW1
VhpAdj
OUT1
cnt1
SW
IN
1609
SWITCH
R1611
V1
1613
vdc=Vcm
gnd

FIG. 17

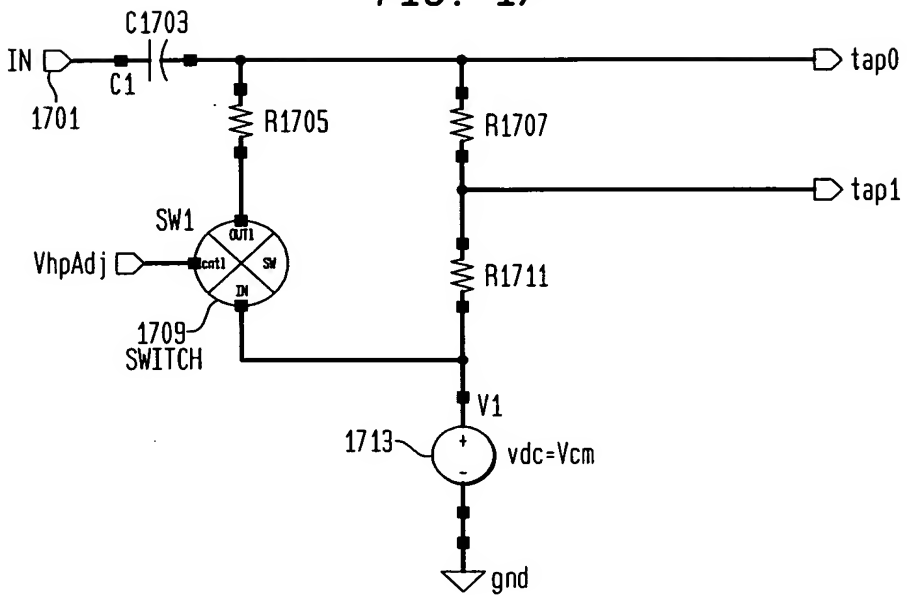

C1703
IN
C1
1701
R1705
R1707
tap0
tap1
SW1
OUT1
cntl
SW
IN
VhpAdj
R1711
1709
SWITCH
V1
1713
vdc=Vcm
gnd

FIG. 18

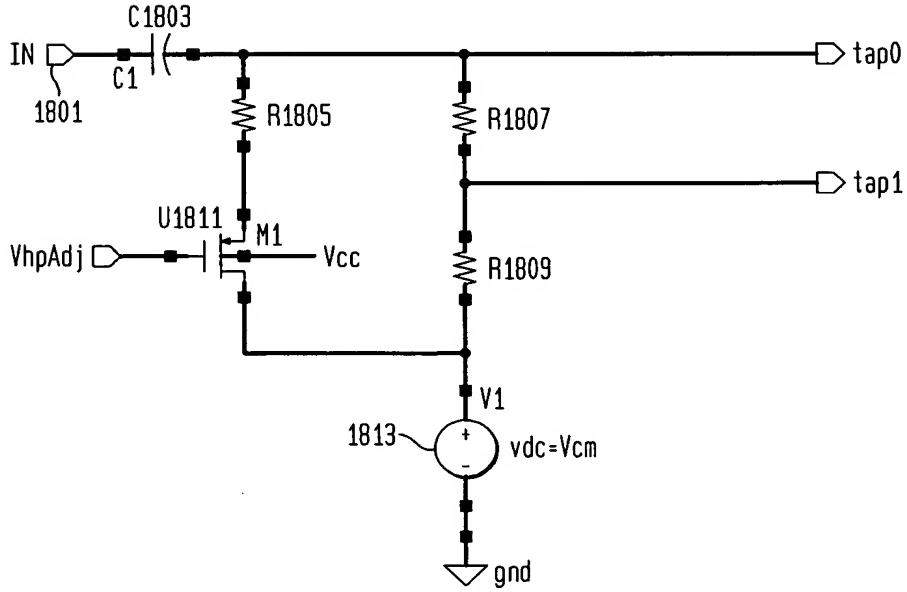
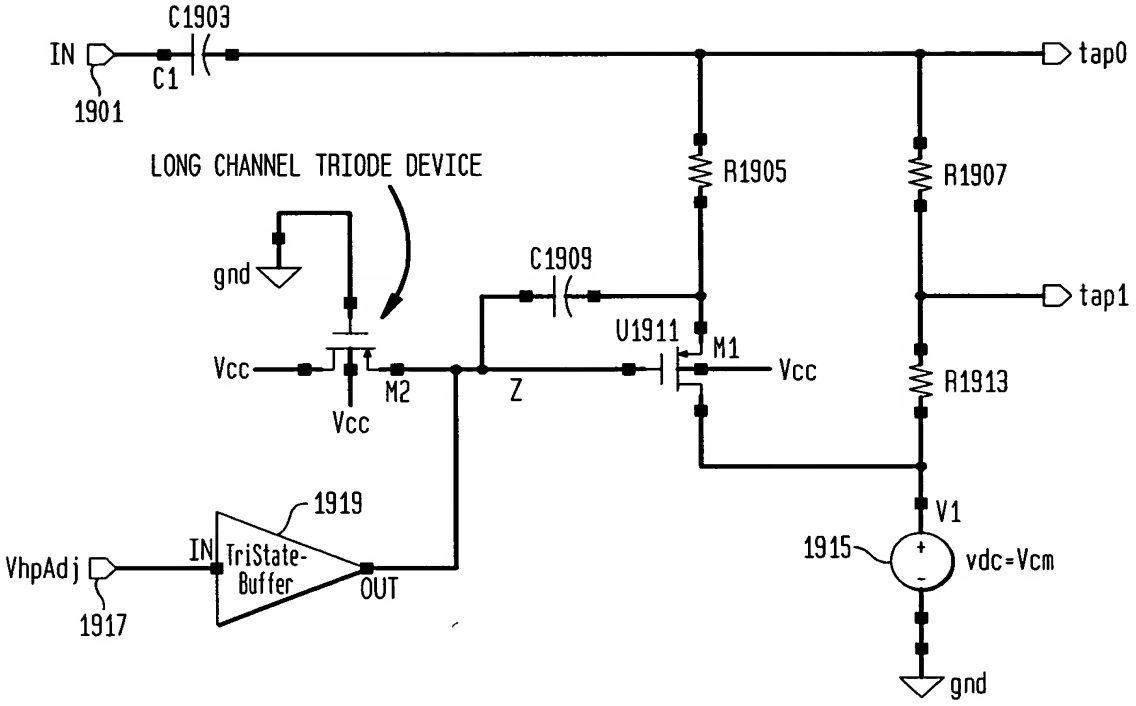

C1803
IN
C1
1801
R1805
R1807
tap0
tap1
U1811
M1
VhpAdj
Vcc
R1809
V1
1813
vdc=Vcm
gnd

FIG. 19


C1903
IN
C1
1901
tap0
LONG CHANNEL TRIODE DEVICE
R1905
R1907
gnd
C1909
tap1
U1911
M1
Vcc
Vcc
M2
Z
Vcc
R1913
1919
V1
1915
vdc=Vcm
VhpAdj
IN
TriState-
Buffer
OUT
1917
gnd

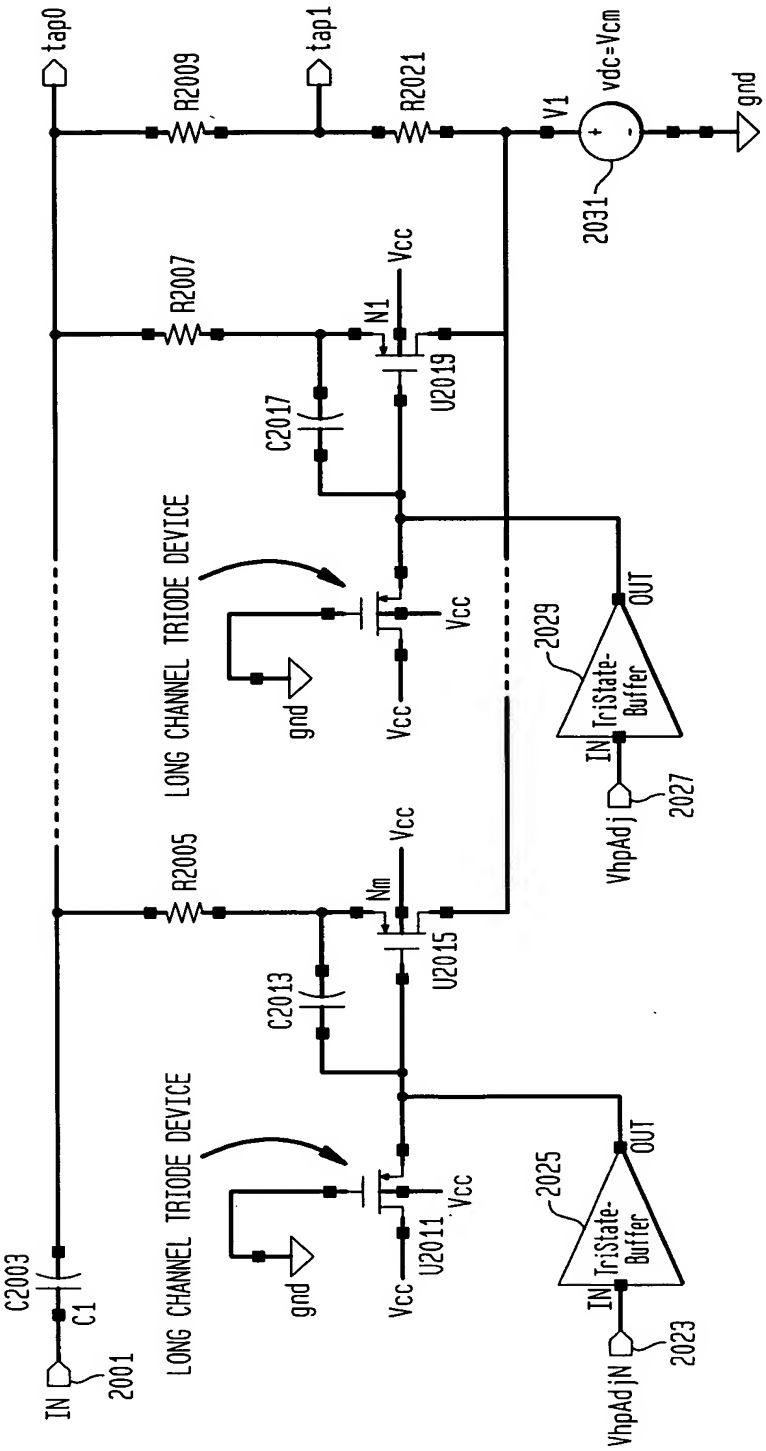

tap0
R2009
tap1
R2021
V1
vdc=Vcm
gnd
2031
R2007
N1
Vcc
U2019
C2017
LONG CHANNEL TRIODE DEVICE
gnd
Vcc
Vcc
2029
TriState-Buffer
IN
OUT
VhpAdj
2027
R2005
Nm
Vcc
U2015
C2013
LONG CHANNEL TRIODE DEVICE
gnd
Vcc
U2011
Vcc
2025
TriState-Buffer
IN
OUT
C2003
C1
IN
2001
VhpAdjN
2023

FIG. 20

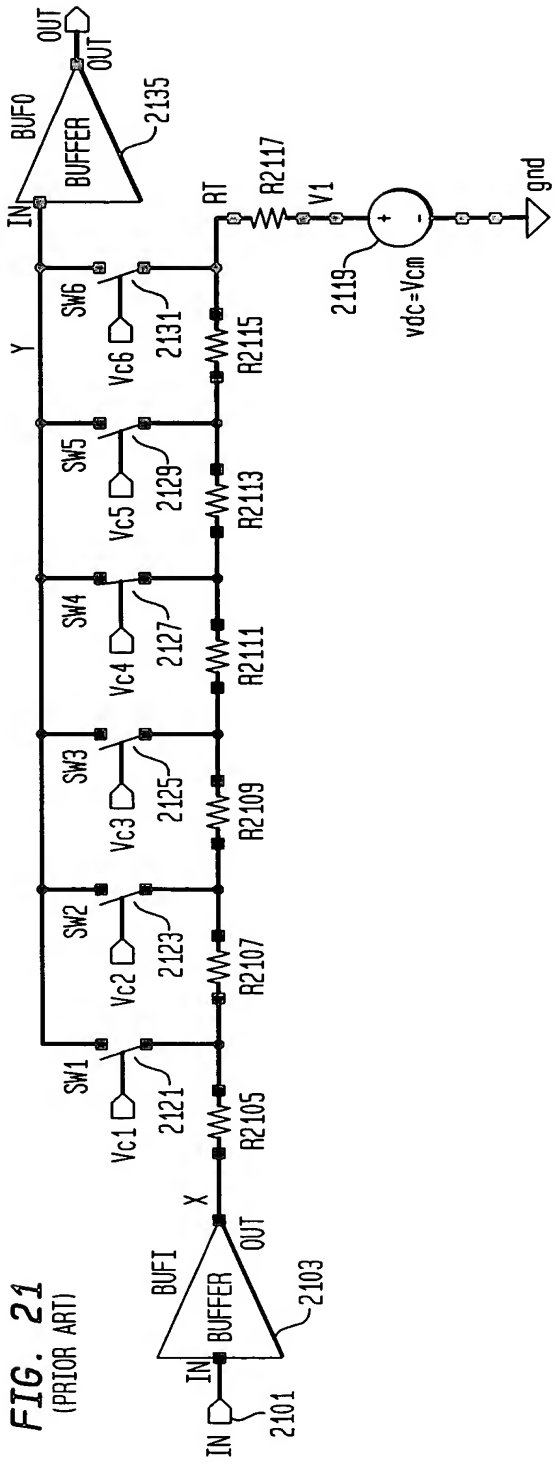


FIG. 21
(PRIOR ART)

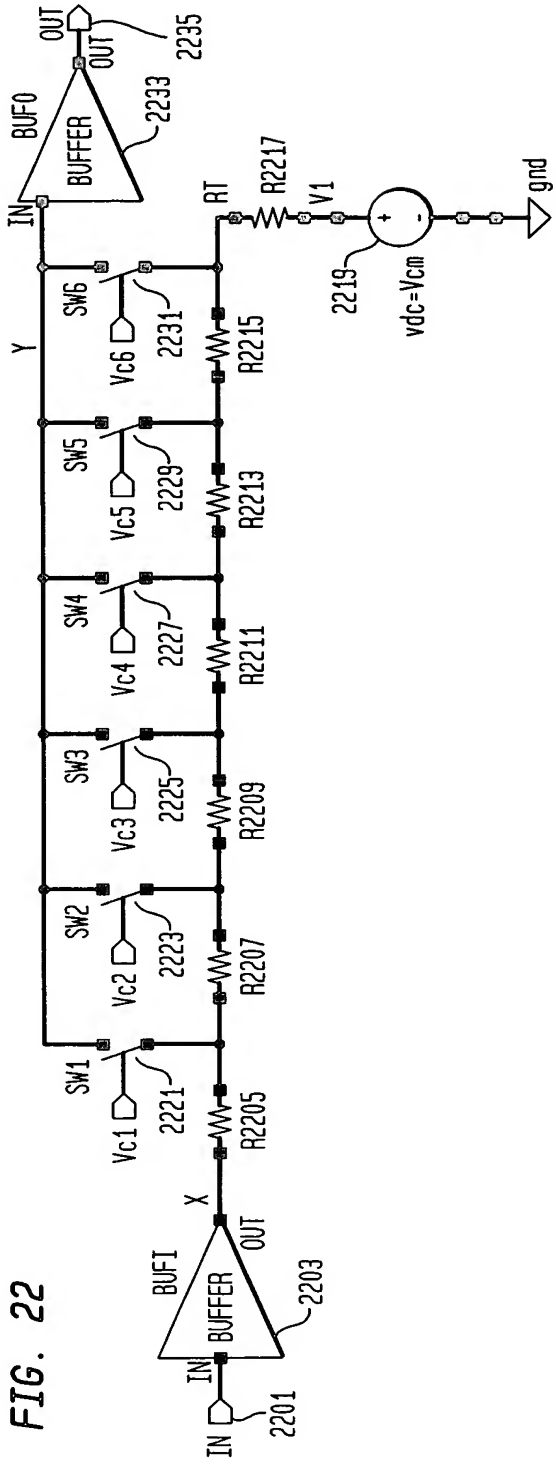


FIG. 22

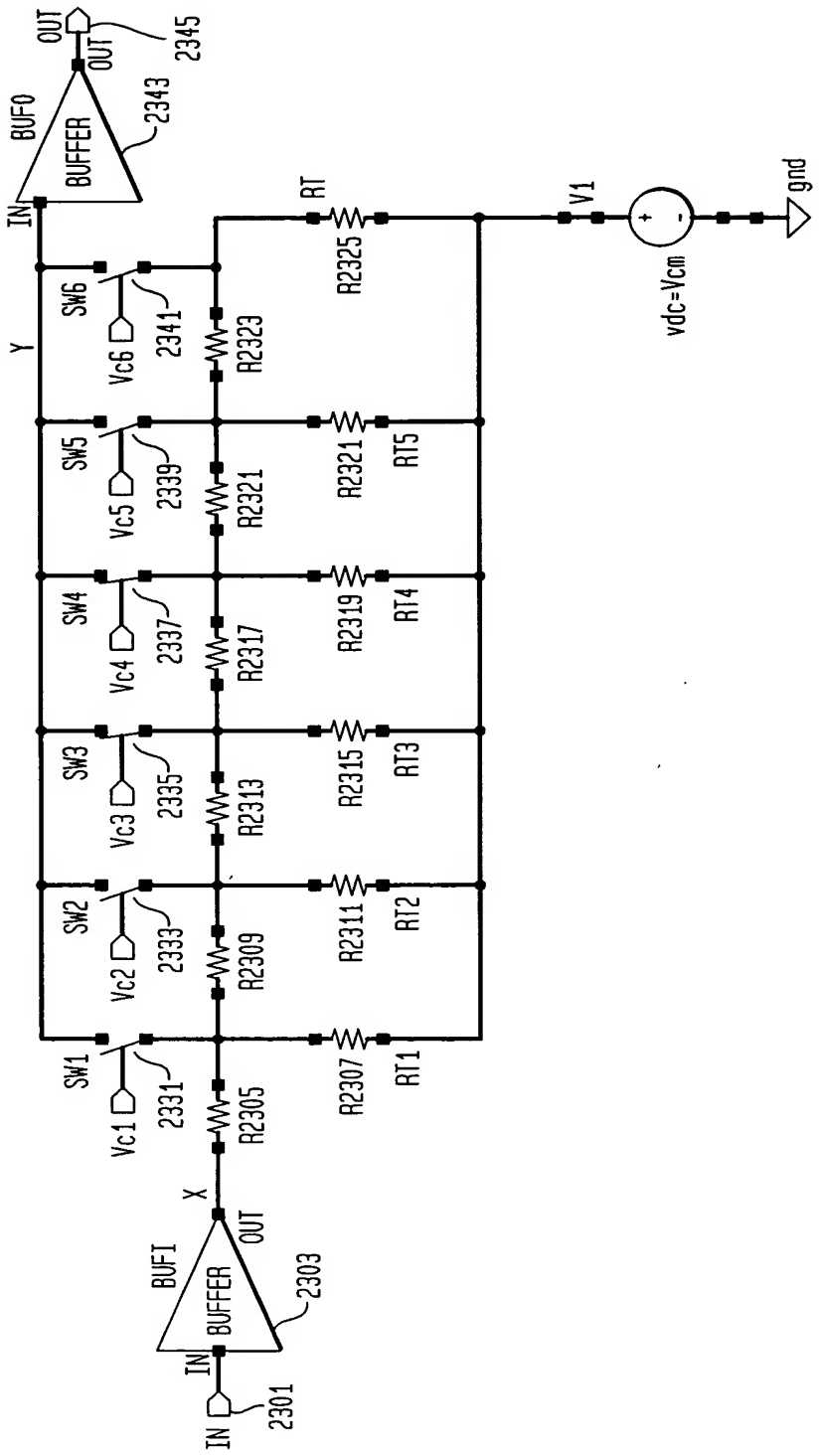

OUT
OUT
2345
BUF0
BUFFER
2343
IN
RT
R2325
V1
gnd
vdc=Vcm
Y
SW6
Vc6
2341
R2323
SW5
Vc5
2339
R2321
R2321
RT5
SW4
Vc4
2337
R2317
R2319
RT4
SW3
Vc3
2335
R2313
R2315
RT3
SW2
Vc2
2333
R2309
R2311
RT2
SW1
Vc1
2331
R2305
R2307
RT1
X
BUFI
OUT
BUFFER
2303
IN
IN
2301

FIG. 23

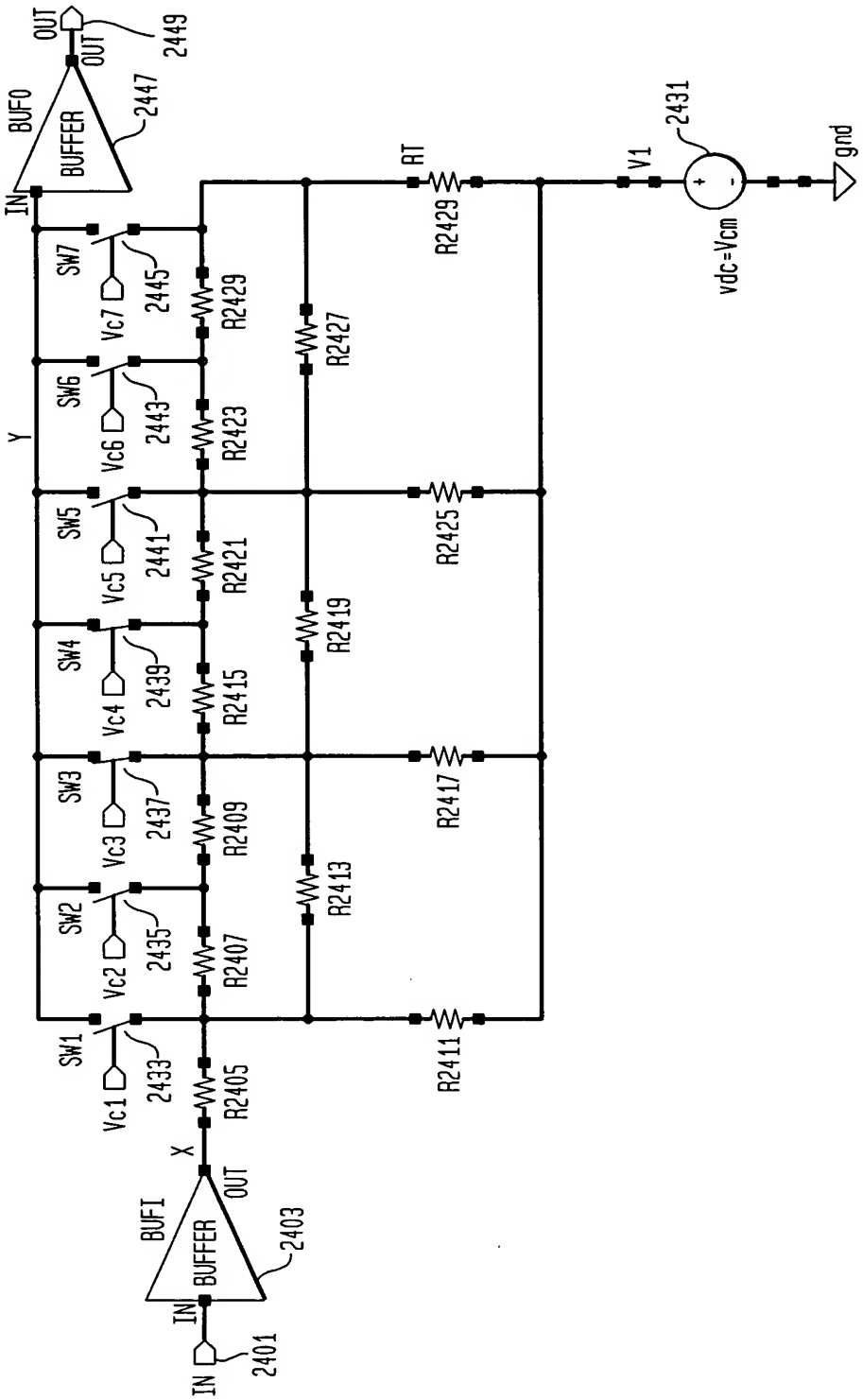
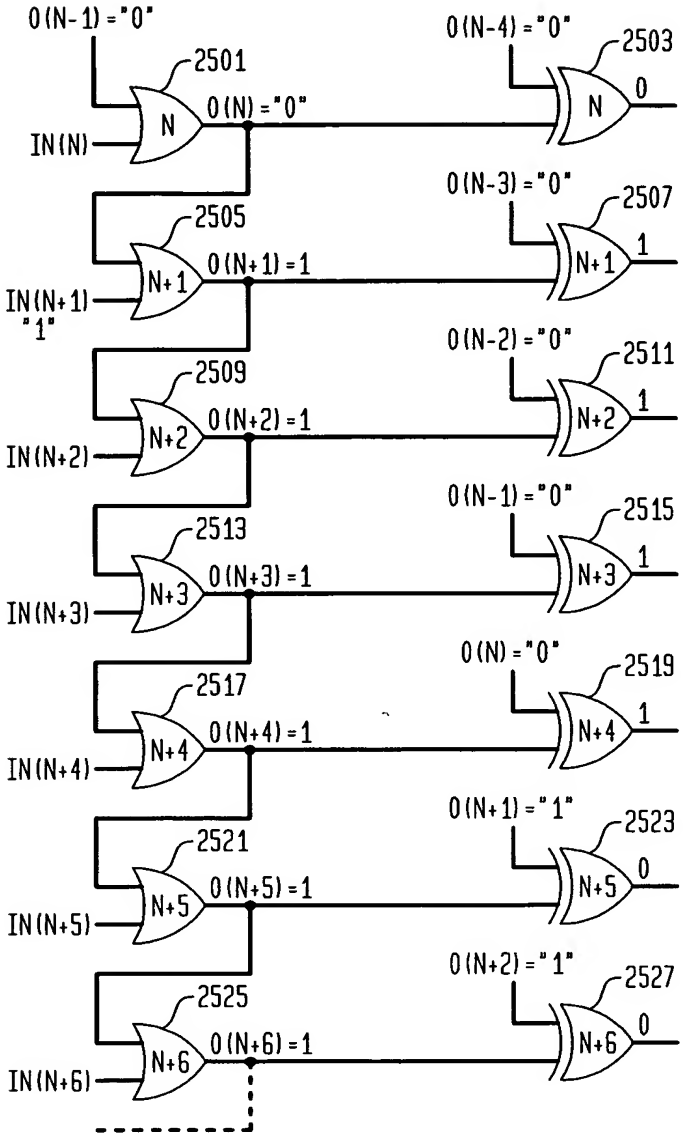

OUT
OUT
2449
BUF0
BUFFER
2447
IN
RT
R2429
V1
2431
gnd
vdc=Vcm
SW7
Vc7
2445
R2429
R2427
SW6
Vc6
2443
R2423
Y
SW5
Vc5
2441
R2421
R2425
SW4
Vc4
2439
R2415
R2419
SW3
Vc3
2437
R2409
R2417
SW2
Vc2
2435
R2407
R2413
SW1
Vc1
2433
R2405
R2411
X
BUFI
OUT
BUFFER
2403
IN
IN
2401

FIG. 24

FIG. 25


O(N-1) = "0"
2501
N
O(N) = "0"
IN(N)
O(N-4) = "0"
2503
N
0
2505
N+1
O(N+1) = 1
IN(N+1) "1"
O(N-3) = "0"
2507
N+1
1
2509
N+2
O(N+2) = 1
IN(N+2)
O(N-2) = "0"
2511
N+2
1
2513
N+3
O(N+3) = 1
IN(N+3)
O(N-1) = "0"
2515
N+3
1
2517
N+4
O(N+4) = 1
IN(N+4)
O(N) = "0"
2519
N+4
1
2521
N+5
O(N+5) = 1
IN(N+5)
O(N+1) = "1"
2523
N+5
0
2525
N+6
O(N+6) = 1
IN(N+6)
O(N+2) = "1"
2527
N+6
0

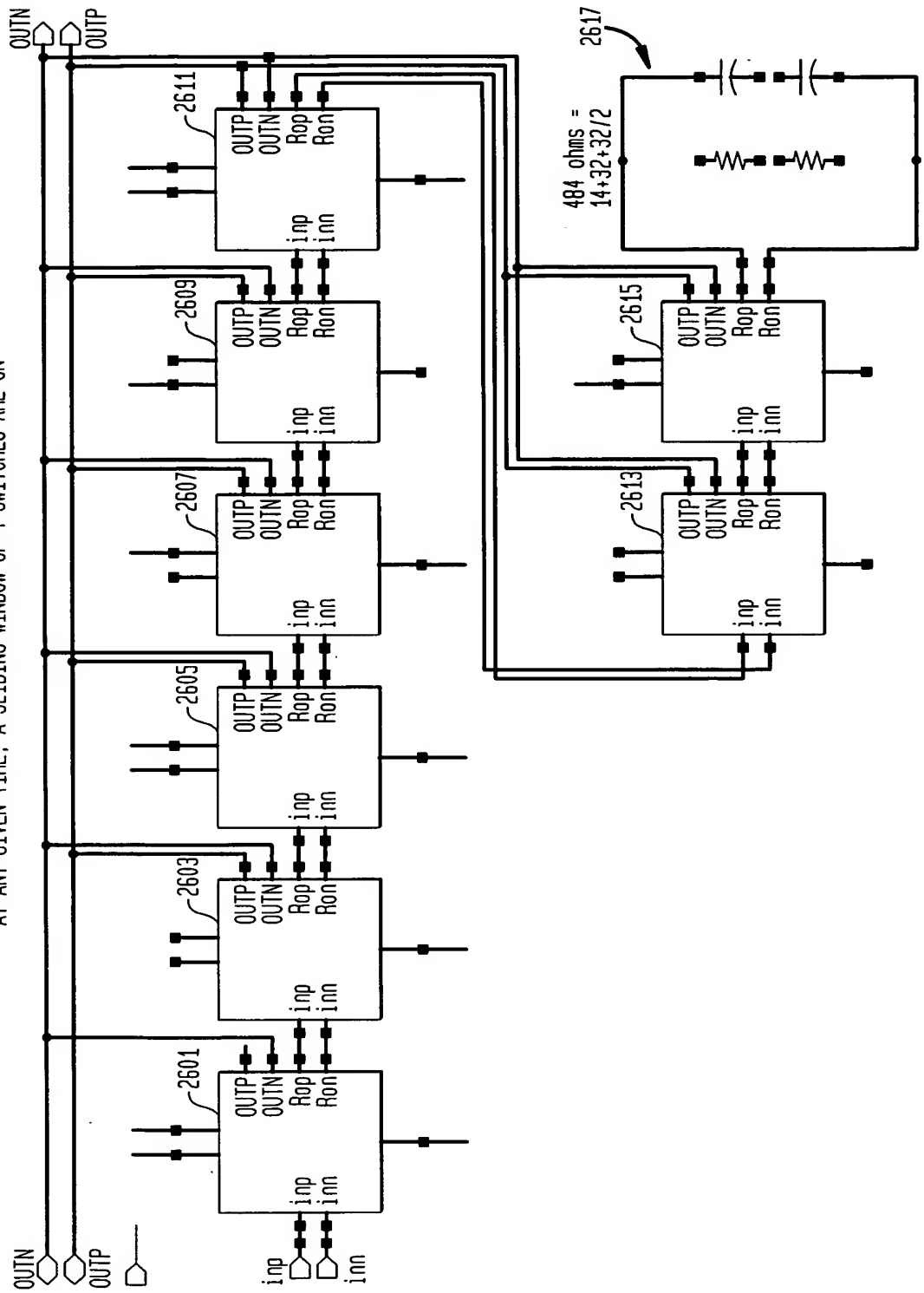


FIG. 26

AT ANY GIVEN TIME, A SLIDING WINDOW OF 4 SWITCHES ARE ON

SWITCH SIZING:
N: w=1.8μ, L=0.25μ, m=2
P: w=2μ, L=0.25 μ m=8

FIG. 27

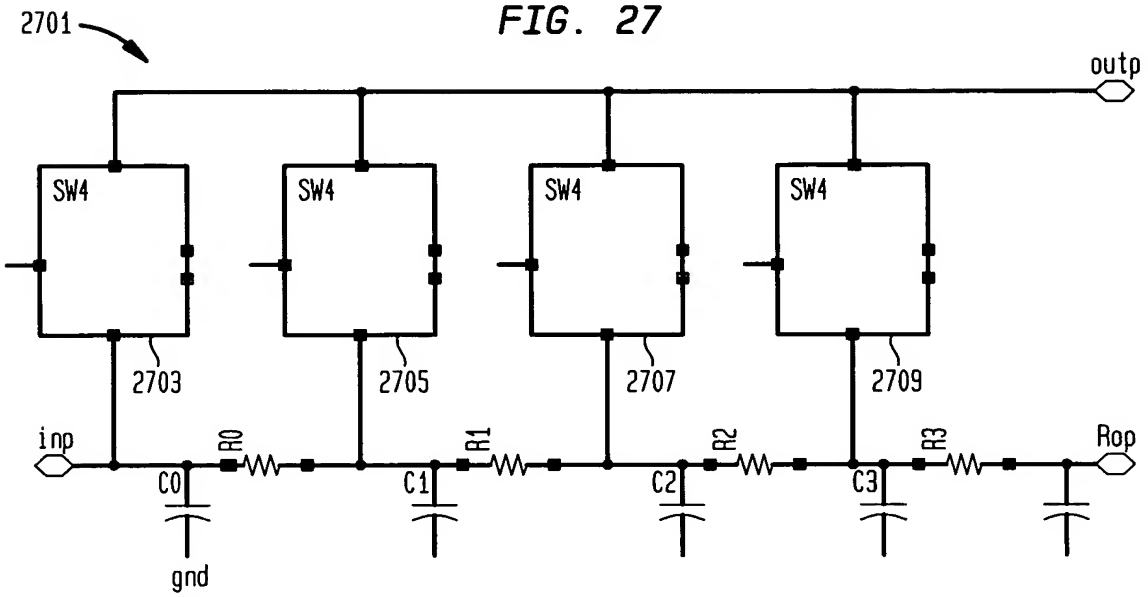


FIG. 28

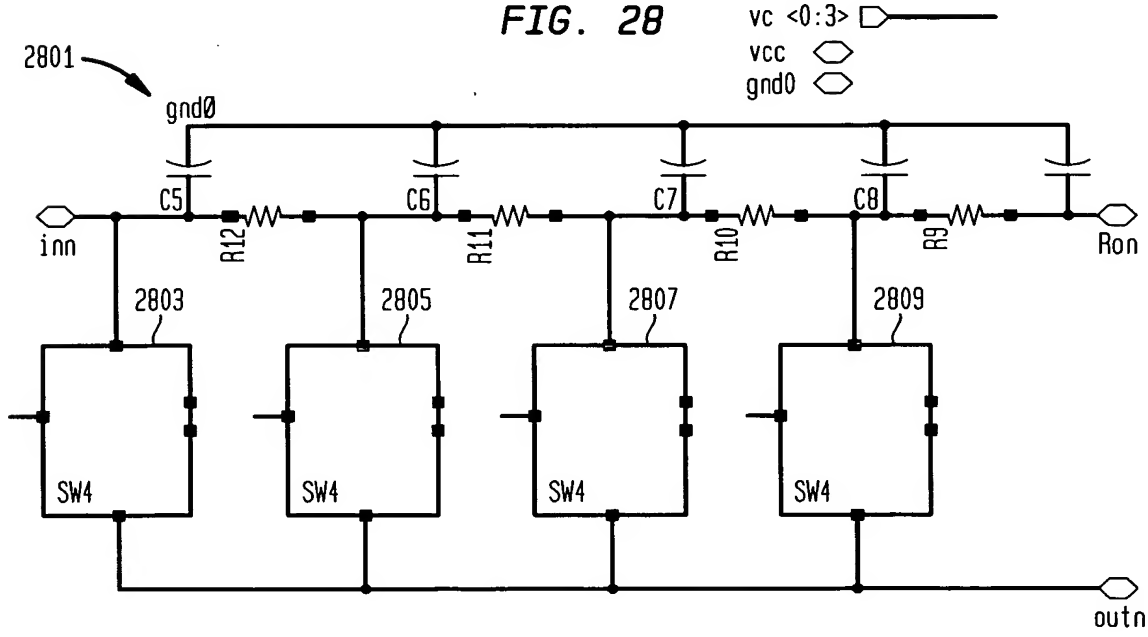
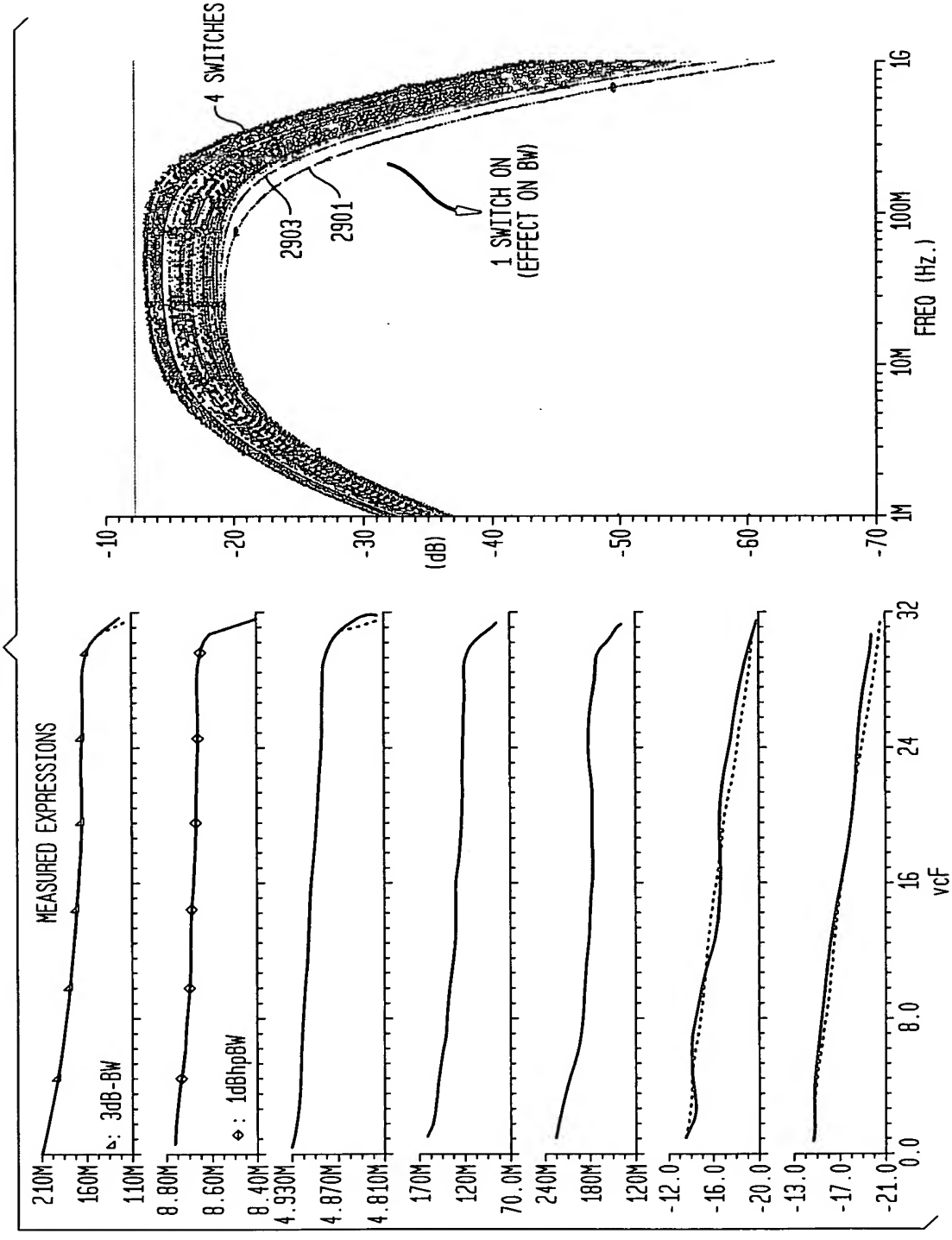


FIG. 29


4 SWITCHES
2903
2901
1 SWITCH ON
(EFFECT ON BW)
-10
-20
-30
-40
-50
-60
-70
(dB)
1M
10M
100M
1G
FREQ (Hz.)
MEASURED EXPRESSIONS
a: 3dB-BW
◇: 1dBhpBW
210M
160M
110M
8.80M
8.60M
8.40M
4.930M
4.870M
4.810M
170M
120M
70.0M
240M
180M
120M
-12.0
-16.0
-20.0
-13.0
-17.0
-21.0
0.0
8.0
16
24
32
VCF

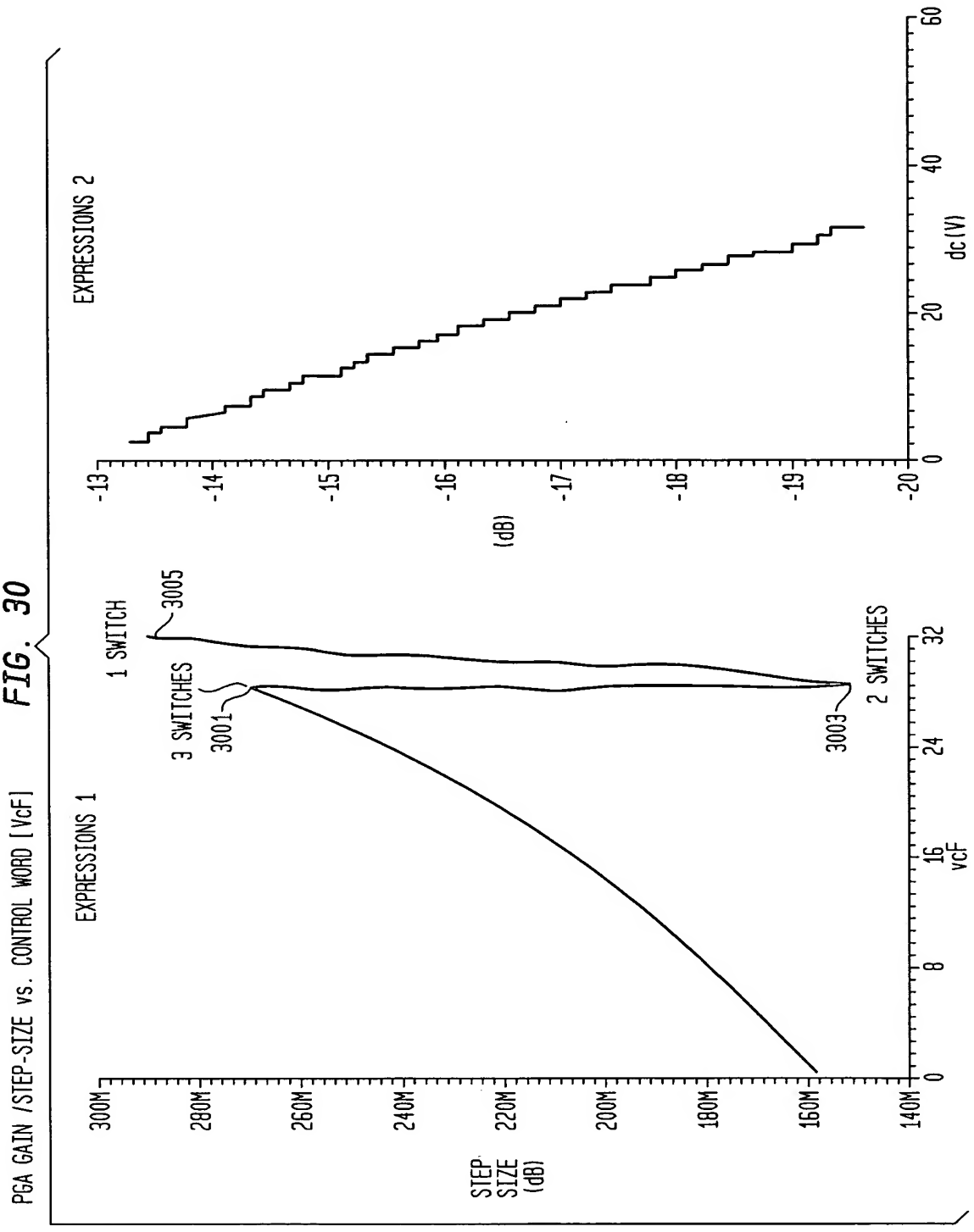

PGA GAIN /STEP-SIZE vs. CONTROL WORD [VcF]
EXPRESSIONS 1
EXPRESSIONS 2
STEP SIZE (dB)
300M
280M
260M
240M
220M
200M
180M
160M
140M
0
8
16
24
32
VcF
1 SWITCH
3005
3 SWITCHES
3001
3003
2 SWITCHES
-13
-14
-15
-16
-17
-18
-19
-20
(dB)
0
20
40
60
dc (V)

FIG. 30

FIG. 31

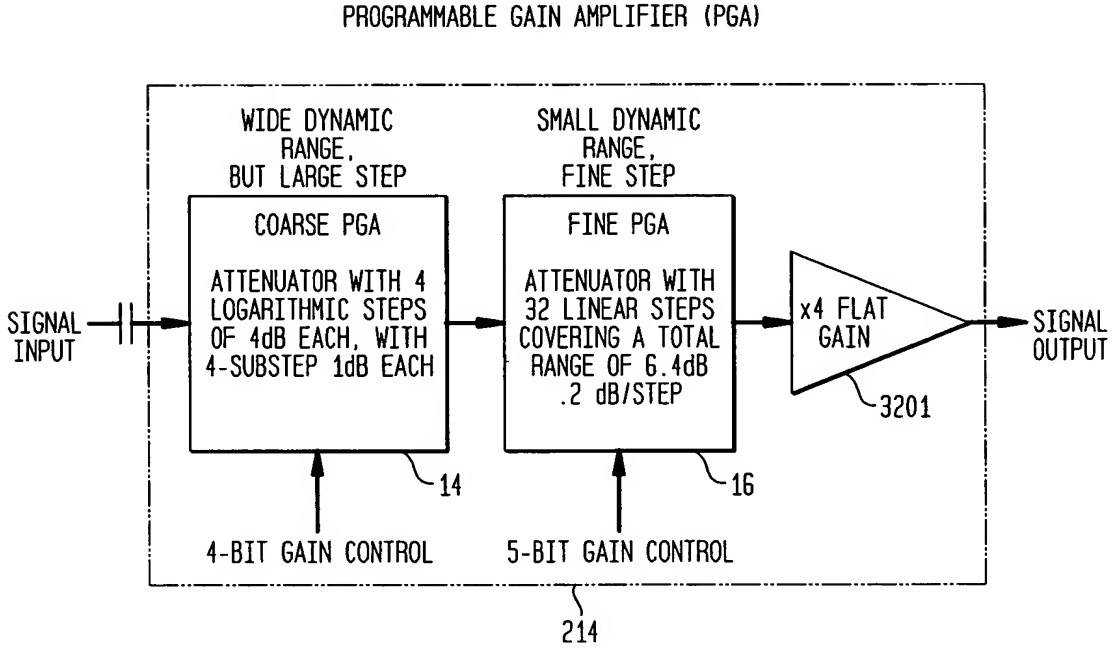
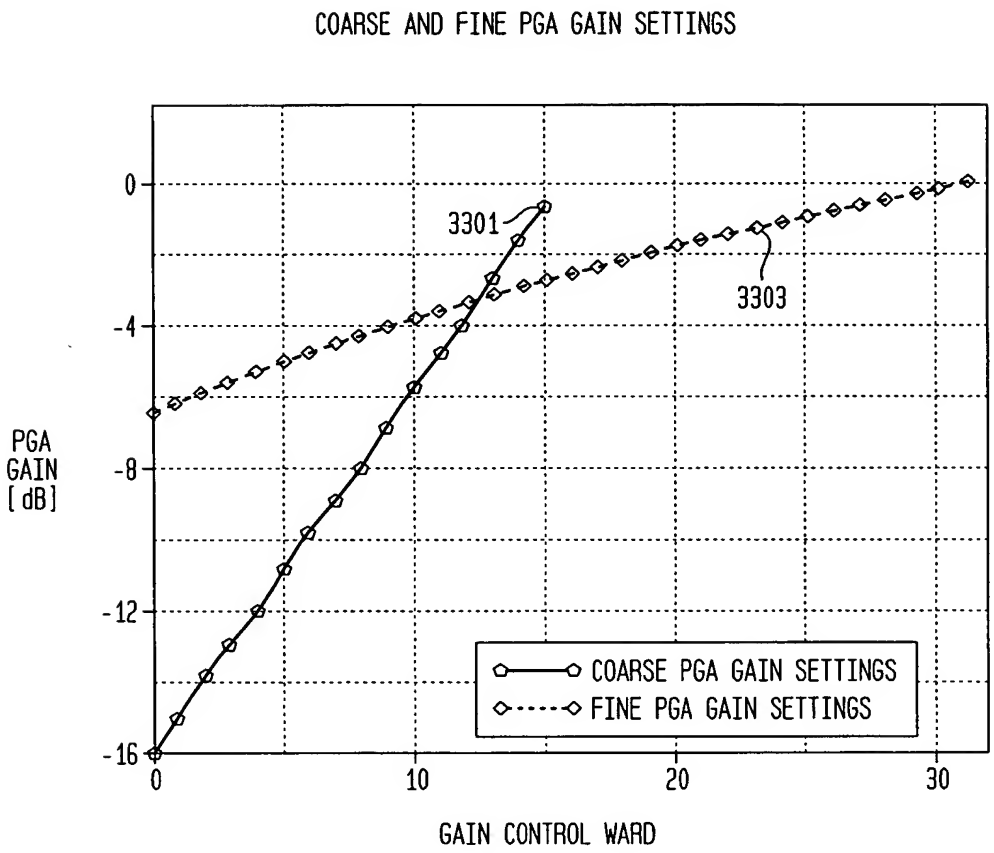

PROGRAMMABLE GAIN AMPLIFIER (PGA)
WIDE DYNAMIC RANGE, BUT LARGE STEP
SMALL DYNAMIC RANGE, FINE STEP
COARSE PGA
ATTENUATOR WITH 4 LOGARITHMIC STEPS OF 4dB EACH, WITH 4-SUBSTEP 1dB EACH
FINE PGA
ATTENUATOR WITH 32 LINEAR STEPS COVERING A TOTAL RANGE OF 6.4dB .2 dB/STEP
x4 FLAT GAIN
3201
SIGNAL INPUT
SIGNAL OUTPUT
14
16
4-BIT GAIN CONTROL
5-BIT GAIN CONTROL
214

FIG. 32


COARSE AND FINE PGA GAIN SETTINGS
PGA GAIN [dB]
0
-4
-8
-12
-16
0
10
20
30
GAIN CONTROL WARD
3301
3303
COARSE PGA GAIN SETTINGS
FINE PGA GAIN SETTINGS

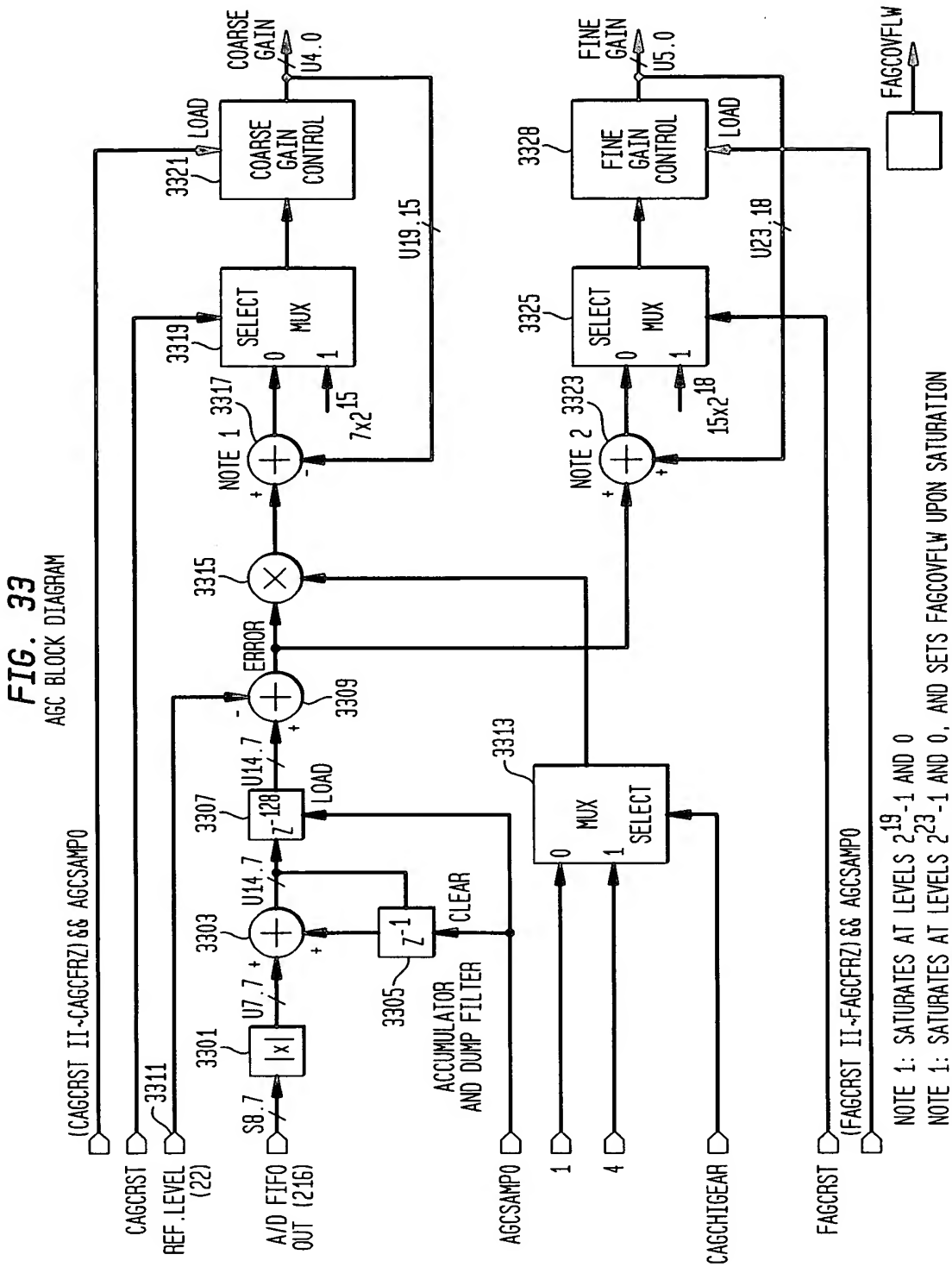


FIG. 33
AGC BLOCK DIAGRAM

NOTE 1: SATURATES AT LEVELS 2^{19}-1 AND 0
NOTE 1: SATURATES AT LEVELS 2^{23}-1 AND 0, AND SETS FAGCOVFLW UPON SATURATION
NOTE 3: FAGCOVFLW IS RESET ONLY BY FAGCRST

FIG. 34

PEAK TO RMS RATIOS FOR 100Base-TX AND GIGABIT

CABLE LENGTH [m]	100Base TX	GIGABIT, 100 OHM	GIGABIT, 85 OHM	GIGABIT, 115 OHM
0	3.691281	4.193192	4.193192	4.193192
20	3.806628	4.501316	4.362110	4.291369
40	3.877284	4.528136	4.457336	4.429949
60	3.894216	4.733644	4.695307	4.646305
80	4.055372	4.878569	4.847844	4.810019
100	4.225522	4.983545	4.991296	4.968900
120	4.357733	5.134131	5.194401	5.154263
140	4.556012	5.266919	5.380943	5.366309
160	4.764462	-	-	-

TARGET E{|x|} = A/D CLIPPING LEVEL x (E{|x|}/RMS)/(PEAK/RMS)
=127 x 0.7979/5.2 = 20